LISTING OF CLAIMS

1. (Previously Presented) A driver circuit for driving a head of a memory disk device, comprising:

switching circuitry connected between a first voltage supply, a second voltage supply and first and second terminals of the head, the switching circuitry including first and second steady state switch-connected resistances each connected at one end to a corresponding one of the first and second terminals and connected at another end to a voltage reference; and

timing circuitry connected to the switching circuitry for connecting the first terminal to a first voltage level during a first time period and to a second voltage level during a second time period following the first time period while disconnecting the first and second steady state switch connected resistances, and connecting the second terminal to a third voltage level during the first time period and to a fourth voltage level during the second time period while disconnecting the first and second steady state switch connected resistances, the first and second time periods occurring when current through the head transitions between steady state current levels, and the first, second, third and fourth voltage levels forming drive signals applied to the head having substantially no common mode voltage.

2. (Original) The circuit of claim 1, further comprising:

a first current source coupled to the first terminal so as to selectively source a steady state current thereto; and

a second current source coupled to the first terminal so as to selectively sink a steady state current therefrom, the first and second current sources being separately connected to the first terminal via the switching circuitry when the head is in steady state conditions.

3. (Original) The circuit of claim 2, further comprising:

a third current source coupled to the second terminal so as to selectively source a steady state current thereto; and

a fourth current source coupled to the second terminal so as to selectively sink a steady state current therefrom, the third and fourth current sources being separately connected to the second terminal via the switching circuitry when the head is in steady state conditions.

4. (Original) The circuit of claim 1, wherein the first and fourth voltage levels are the first voltage supply, and the second and third voltage levels are the second voltage supply.

5. (Original) The circuit of claim 1, wherein the second and fourth voltage levels are approximately positive and negative supply voltages.

6. (Original) The circuit of claim 1, wherein the first voltage level is the first voltage supply and the second voltage level is the second voltage supply.

7. (Original) The circuit of claim 1, wherein the first time period is approximately the time it takes for the current flowing through the head to transition from a first steady state current level to an overshoot current level having a greater magnitude than a second steady state current level.

8. (Currently Amended) The circuit of claim 7, wherein the second time period is approximately the time it takes for the current flowing through the head to transition from the ~~first~~ overshoot current level to an undershoot current level having a lesser magnitude than the second steady state current level.

9. (Previously Presented) A driver circuit for driving a head of a memory disk device, comprising:

switching circuitry connected between a first voltage supply, a second voltage supply and first and second terminals of opposite ends of a write coil;

timing circuitry connected to the switching circuitry for connecting the first terminal to a first voltage level during a first time period and to a second voltage level during a second time period following the first time period, and connecting the second terminal to a third voltage level during the first time period and to a fourth voltage level during the second time period, the first and second time periods occurring when current through the head transitions between steady state current levels;

a first resistance element connected at one end to the first terminal and at another end to a ground reference; and

a second resistance element connected at one end to the second terminal and at another end to the ground reference.

10. (Previously Presented) A driver circuit for driving a head of a memory disk device, comprising:

switching circuitry connected between a first voltage supply, a second voltage supply and first and second terminals of the head;

timing circuitry connected to the switching circuitry for connecting the first terminal to a first voltage level during a first time period and to a second voltage level during a second time period following the first time period, and connecting the second terminal to a third voltage level during the first time period and to a fourth voltage level during the second time period, the first and second time periods occurring when current through the head transitions between steady state current levels, and the first, second, third and fourth voltage levels forming drive signals applied to the head having substantially no common mode voltage;

a first resistance element connected between the first terminal and a ground reference; and

a second resistance element connected between the second terminal and the ground reference;

wherein the first and second resistive elements are variable resistance elements.

11. (Original) The circuit of claim 9, wherein the first and second resistance elements are disconnected from the first and second terminals, respectively, during the first and second time periods.

12. (Original) The circuit of claim 1, wherein the timing circuitry provides control signals to the switching circuitry, the control signals having a minimum pulse width approximately equal to the reciprocal of the data rate of the memory disk device.

13. (Original) The circuit of claim 1, further comprising:

a first current source connected between the first voltage supply and the first terminal; and

a second current source connected between the first terminal and the second voltage supply, wherein the timing circuitry selectively allows the first current source to source current to the first terminal when the head is in a first steady state, and selectively allows the second current source to sink current from the first terminal when the head is in a second steady state.

14. (Original) The circuit of claim 13, wherein the switching circuitry and the timing circuitry selectively provide current paths to the first terminal during the first and second time periods that are in parallel with current paths formed by the first and second current sources

15. (Original) The circuit of claim 1, wherein the head is the write head of a disk drive.

16. (Previously Presented) A method of driving a head of a magnetic disk memory device which includes a first terminal and second terminal, the first terminal connected to a reference voltage through a first steady state switch connected resistance and the second terminal connected to the reference voltage through a second steady state switch connected resistance, comprising:

sourcing a first steady state current level to a first terminal of the head and sinking the first steady state current level from a second terminal of the head while the first and second steady state resistances are connected;

driving, during a first time period, the first terminal of the head to a first voltage level and driving the second terminal to a second voltage level so as to reverse the direction of current flow in the head while the first and second steady state resistances are disconnected;

driving, during a second time period following the first time period, the first terminal of the head to a third voltage level and driving the second terminal to a fourth voltage level while the first and second steady state resistances are disconnected, the first, second, third and fourth voltage levels forming drive signals for the head having approximately zero common mode voltage; and

following the second period of time, sinking the first steady state current level from the first terminal and sourcing the first steady state current level to the second terminal while the first and second steady state resistances are connected.

17. (Original) The method of claim 16, wherein:

the first and fourth voltage levels are the same, and the second and third voltage levels are the same.

18. (Original) The method of claim 16, wherein:

the first and fourth voltage levels are a first voltage supply level, and the second and third voltage levels are a second voltage supply level.

19. (Original) The method of claim 16, wherein:

the third and fourth voltage levels are approximately at opposite voltage supplies, and the first and second voltage levels have substantially the same magnitude.

20. (Original) The method of claim 16, wherein the first time period is approximately the time for the current flowing through the head to transition from the first steady state current level to an overshoot current level having a magnitude greater than the second current level.

21. (Original) The method of claim 20, wherein the second time period is approximately the time for the current flowing through the head to transition from the overshoot current level to a predetermined undershoot current level having a magnitude less than the second steady state current level.

22. (Previously Presented) An apparatus, comprising

a disk drive, comprising:

at least one disk on which data is stored;

a spindle motor and controller therefor, the spindle motor being operably connected to the at least one disk;

a read head positioned proximally to the at least one disk;

read channel circuitry, coupled to the read head, for converting signals received on the read head;

a write head positioned proximally to the at least one disk and including a first terminal and a second terminal, the first terminal connected to a reference voltage through a first steady state switch connected resistance and the second terminal connected to the reference voltage through a second steady state switch connected resistance; and

write channel circuitry, coupled to the first and second terminals of the write head, for applying drive signals to the first and second terminals of the write head corresponding to data to be written onto the at least one disk, and for disconnecting the first and second steady state resistances during the time current in the write head transitions between steady state current levels.

23. (Original) The apparatus of claim 22, wherein the first and second terminals are connected to opposite supply voltage levels during a first portion of the time a current in the write head transitions between steady state current levels, and the voltage supply levels connected to the first and second terminals are reversed during a second portion of the time the current in the write head transitions between steady state current levels.

24. (Original) A disk drive, comprising:

at least one disk on which data is stored;

a spindle motor and controller therefor, the spindle motor being operably connected to the at least one disk;

a read head positioned proximally to the at least one disk;

read channel circuitry, coupled to the read head, for converting signals received on the read head;

a write head positioned proximally to the at least one disk and including a first terminal and a second terminal; and

write channel circuitry, coupled to the first and second terminals of the write head, for applying drive signals to the first and second terminals of the write head corresponding to data to be written onto the at least one disk, comprising:

a plurality of switching transistors, connected between a first voltage supply, a second voltage supply and first and second terminals of the write head;

a plurality of current sources connected between the first and second voltage supplies and the write head; and

timing circuitry, connected to the switching circuitry and the current source, for generating control signals for selectively activating the switching transistors and the current sources, the minimum pulsewidth appearing on the control signals being an inverse of the rate at which data is written on the disk.